CLAIMS

What is claimed is:

1. A method, comprising:

assigning a plurality of nodes within a storage circuit to a predetermined state;

evaluating a plurality of signals coupled to the storage circuit, wherein evaluating the plurality of signals enables a first node to change from its predetermined state and enables a second node to be more susceptible to perturbations; and

maintaining the second node in its predetermined state for a predetermined period of time, wherein maintaining the predetermined state reduces the storage circuit's susceptibility to soft errors.

2. The method of claim 1, further comprising disabling a clock signal within the plurality of signals during a pre-charge phase.

3. The method of claim 2, further comprising configuring an input signal within the plurality of signals during the pre-charge phase of the clock signal.

4. The method of claim 1, further comprising enabling a clock signal during an evaluate phase.

5. The method of claim 4, further comprising relating the predetermined period of time to the beginning of the evaluate phase of the clock signal.

6. The method of claim 1, further comprising delaying a signal propagation between the first and second nodes using a plurality of inverters.

7. The method of claim 1, further comprising maintaining the second node at its predetermined state using a plurality of transistors.

8. The method of claim 7, wherein the plurality of transistors couple to the second node and also couple to a voltage source.

9. The method of claim 1, further comprising maintaining the second node at their predetermined states using active pull-up techniques.

10. A storage circuit comprising:

a plurality of nodes including a first node and a second node, wherein the second node is coupled to the first node;

a plurality of signals coupled to the storage circuit, wherein the signals enable a first node to change from a predetermined state; and

a circuit element coupled to the second node, wherein the circuit element maintains the second node in its predetermined state for a predetermined period of time.

11. The storage circuit of claim 10, wherein the circuit element further comprises metal oxide semiconductor field effect transistors ("MOSFETs").

12. The storage circuit of claim 11, wherein the size of the transistors is varied to vary the period of time that the second node is maintained in the predetermined state.

13. The storage circuit of claim 10, wherein an inverter is coupled between the first node and the second node.

14. The storage circuit of claim 10, further comprising a plurality of inverters coupled between the first and second nodes.

15. The storage circuit of claim 10, wherein the timing signal comprises a pre-charge phase and an evaluate phase, and wherein the nodes are set high during the pre-charge phase, and wherein the nodes are set to a finalized state during the evaluate phase.

16. A computer system, comprising:

a processor;

a system memory coupled to said processor, wherein the memory further comprises:

a plurality of nodes;

a timing signal; and

at least one control signal;

wherein the timing signal and the control signals cause a first node within the plurality to change from an initialized state to a finalized state while a second node within the plurality is maintained in an initialized state; and

wherein maintaining the second node while the first node is changing reduces the storage circuit's susceptibility to soft errors.

17. The computer system of claim 16, wherein the timing signal comprises a pre-charge phase and an evaluate phase.

18. The computer of claim 17, wherein the first and second nodes are initialized during the pre-charge phase, and the first node is changed from the initialized state to a second state during the evaluate phase, and wherein the second node is maintained in the initialized state for at least a portion of the evaluate phase.

19. The computer of claim 17, wherein the at least one signal is configured during the pre-charge phase.

20. A storage circuit, comprising:

a means for enabling and disabling a clock signal, wherein the means for enabling and disabling enables a plurality of nodes in the storage circuit to be assigned a predetermined state and wherein the

means for enabling and disabling enables a first node within the plurality of nodes to change states; and

a means for maintaining a second node within the plurality of nodes at a predetermined state while the first node is changing states, wherein the means for maintaining the second node at a predetermined state reduces the storage circuit's susceptibility to soft errors.

21. The storage circuit of claim 20, further comprising means for configuring an input signal and a clock signal.

22. The storage circuit of claim 21, wherein the clock signal comprises a pre-charge phase and an evaluate phase and the input signal is configured during the pre-charge phase and the first node changes states during the evaluate phase and the second node is maintained at its predetermined state during the evaluate phase.